PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2002-299607

(43)Date of publication of application : 11.10.2002

(51)Int.Cl. H01L 29/78
H01L 21/283
H01L 21/318

(21)Application number : 2001-094052

(22)Date of filing : 28.03.2001

(71)Applicant : TOSHIBA CORP

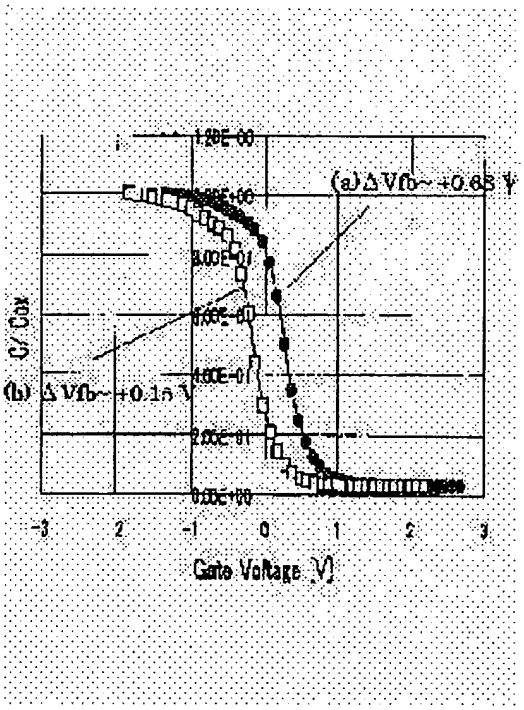
(72)Inventor : YAMAGUCHI TAKESHI
SATAKE HIDEKI
FUKUSHIMA SHIN

(54) MISFET AND METHOD OF MANUFACTURING THE SAME

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a MISFET (metal insulator semiconductor field effect transistor) which is capable of preventing the diffusion of impurities and metal atoms from a gate electrode even if a metal oxide which can earn a physical film thickness is used as a gate insulation film, and is also capable of suppressing the decrease in flat band voltage shift and mobility, and also to provide a method of manufacturing the same.

SOLUTION: The MISFET comprises a silicon substrate 101, a gate insulation film 103 which is formed of a metal oxide and includes nitrogen at least in a part of it and is formed on the silicon substrate 101, and a gate electrode 104 formed on the gate insulation film 103. In the gate insulation film 103, the content of nitrogen near an interface with the silicon substrate is higher than that in the other parts.



LEGAL STATUS

[Date of request for examination] 25.02.2003

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] It is related with an MIS mold field-effect transistor and this manufacture approach.
[0002]
[Description of the Prior Art] In order to accelerate a semiconductor integrated circuit (LSI) and to be integrated highly to current, it has been advanced by detailed-ization of the MIS mold field-effect transistor in accordance with a scaling law. An insulator layer, gate die length, etc. of an MIS mold field-effect transistor are reducing the dimension of the height direction of a component, and a longitudinal direction to coincidence, and a scaling law is the approach of keeping a switching characteristic normal and attaining improvement in the speed and high integration.
[0003] According to this scaling law, the next-generation MIS mold field-effect transistor in A.D. 2001 and afterwards requires the capacity by which gate-dielectric-film capacity converts into SiO2, and is equivalent to 2nm or less in thickness. However, in SiO2 conventionally used as gate dielectric film, direct tunnel current flows by 2nm or less in thickness, and control of leakage current cannot be performed, but problems, such as an increment in power consumption, arise.
[0004] So, to earn physical thickness and to suppress leakage current is tried by the next-generation MIS mold field-effect transistor, holding down silicon oxide conversion effective thickness to 2nm or less using an ingredient with a dielectric constant higher than SiO2 as gate dielectric film.
[0005] Moreover, in an MIS mold field-effect transistor, leakage current is controlled, and also it runs, and there is a problem of an electrical potential difference. It runs, and an electrical potential difference is a problem on which impurities, such as Lynn (P) which is the dopant of polycrystalline silicon, and boron (B), run through gate dielectric film, it is spread all over a channel field, and threshold voltage is changed with this impurity, when polycrystalline silicon is used for a gate electrode. By generating heat, while operating the component, since an impurity is spread and a threshold changes as time amount is formed, this phenomenon has the problem that dependability deteriorates.
[0006] Using a metal for a gate electrode is examined by the next-generation MIS transistor as this approach of running and solving the problem of an electrical potential difference, and a means to attain low resistance-ization of a gate electrode. However, if a metal is used for a gate electrode, a metal atom will be spread even in an interface with the inside of gate dielectric film, or a silicon substrate from a gate electrode, a fixed charge will be generated in gate dielectric film, and a flat-band-voltage shift and the fall of mobility will become a problem. Especially, as gate dielectric film, if a metallic oxide is used, since whenever [diffusion / of a metal atom] is very higher than SiO2, many fixed charges will be generated in gate dielectric film, and a metallic oxide will become a very big problem.
[0007]
[Problem(s) to be Solved by the Invention] As mentioned above, in a next-generation MIS field-

effect transistor, there is a technical problem which must be solved variously in a sake advancing detailed-ization.
[0008] This invention was made in view of this trouble, even if the metallic oxide which can earn physical thickness is used for it as gate dielectric film, it becomes possible [preventing diffusion of the impurity metallurgy group atom from a gate electrode], and it aims at offering the MIS mold field-effect transistor which can control a flat-band-voltage shift and the fall of mobility, and its manufacture approach.
[0009]
[Means for Solving the Problem] By this invention, the electrical characteristics of a transistor are raised by preventing diffusion of the impurity metallurgy group from a gate electrode, and not making coincidence contain nitrogen in an interface with a silicon substrate by making the metallic oxide in gate dielectric film contain nitrogen.
[0010] Then, this invention The gate dielectric film which becomes at least the part formed on the silicon substrate and said silicon substrate from the metallic-oxide film or metal acid nitride film containing nitrogen, and the gate electrode formed on said gate dielectric film are provided, and the MIS mold field-effect transistor characterized by the nitrogen content near the interface with said silicon substrate being lower than other parts of said gate dielectric film among said metallic-oxide film or the metal acid nitride film is offered.
[0011] At this time, it is desirable that the nitrogen content near the interface with said silicon substrate is less than [0.1atomic%] among said gate dielectric film.
[0012] Moreover, it is desirable that it is 0.6nm or less in thickness near the interface with said silicon substrate from said silicon substrate among said gate dielectric film.
[0013] Moreover, it is desirable that a nitrogen content with a thickness [an interface with said gate electrode to] of 0.6nm or less is more than 10atomic% among said gate dielectric film.
[0014] Moreover, the gate dielectric film with which this invention becomes at least the part formed on the silicon substrate and said silicon substrate from the metallic oxide containing nitrogen, The gate electrode formed on said gate dielectric film is provided, and the nitrogen content in a field with a thickness of 0.6nm is less than [0.1atomic%] from an interface with said silicon substrate among said gate dielectric film. And the MIS mold field-effect transistor characterized by the nitrogen content in a field with a thickness of 0.6nm being more than 10atomic% at least is offered from an interface with said gate electrode among said gate dielectric film.
[0015] At this time, it is desirable that silicon contains in said gate dielectric film.
[0016] Moreover, this invention offers the MIS mold field-effect transistor characterized by providing a silicon substrate, the gate dielectric film which consists of a metallic oxide formed on said silicon substrate, the silicon nitride formed on said gate dielectric film, and the gate electrode formed on said silicon nitride.
[0017] As for said metallic oxide, at this time, it is desirable that Zr, Hf, La, Ce, Ti, aluminum, Y, Mg, Ta, or Bi is included. It is the case where Zr, Hf, La, Ce, Y, Mg, Ta, or Bi is included especially desirably.
[0018] Moreover, it is desirable by being exposed into heat treatment or excitation nitrogen in nitrogen-gas-atmosphere mind to introduce nitrogen into said metallic oxide.
[0019] Moreover, before forming said gate electrode, it is desirable by being exposed into heat treatment or excitation nitrogen in nitrogen-gas-atmosphere mind to introduce nitrogen into said metallic oxide.
[0020]
[Embodiment of the Invention] First, whenever [diffusion-at 800 to 1200 degrees C of boron (B)] is shown as an impurity in the inside of AlN which is the insulator layer which contains nitrogen in below with aluminum 2O3 as a metallic oxide.
whenever [in / B / aluminum2O3 film / diffusion] -- (800 degrees C - 1200 degrees C) diffusion [of B in the =2 - 6x10-5AlN film] whenever (800 degrees C - 1200 degrees C) = -- one to 6x10-6 -- compared with the insulator layer in which the insulator layer which contains nitrogen in this way

does not contain nitrogen, whenever [diffusion / of an impurity] is small enough.
[0021] Moreover, the 1700-degree C diffusion coefficient of aluminum3+ is indicated to be aluminum 2O3 as a metal atom in the inside of AlN as a metal acid nitride as a metallic oxide. diffusion coefficient [of aluminum3+ in aluminum2O3 film] (1700 degrees C) = -- diffusion coefficient (1700 degrees C) =4x10-13 of aluminum3+ in the 1.4x10-11AlN film -- also whenever [diffusion / of a metal atom] is known by that the insulator layer which contains nitrogen in this way is fully small compared with the insulator layer which does not contain nitrogen. So, in this invention, we decided to use as a diffusion barrier layer which prevents diffusion of the element (impurity metallurgy group atom) which constitutes a gate electrode by forming the layer which makes the part in the gate dielectric film which consists of a metal oxide film or a metal acid nitride contain nitrogen.
[0022] Moreover, when the nitrogen concentration in a metal oxide film or a metal acid nitride was raised, whenever [diffusion / of an impurity metallurgy group atom] became smaller, and it turned out that diffusion barrier property improves. However, there is an inclination for a silicon substrate interface property to deteriorate with the charge by which becomes easy to form a defect and the trap was carried out to the defect when nitrogen existed near the silicon substrate interface of gate dielectric film.
[0023] So, it is required for a silicon substrate surface to make it nitrogen serve as super-low concentration. When the experiment was conducted from this viewpoint, in order not to cause degradation of an interface property, it turned out that it is necessary to be a nitrogen content below the limit of detection of general analysis apparatus, such as XPS. Then, the nitrogen content near the interface with a silicon substrate needs to be less than [0.1atomic%] among the gate dielectric film which consists of the metal oxide film or metal acid nitride containing nitrogen in this invention. It is less than [0.01atomic%] more desirably. When improvement in an interface property is furthermore required, it is desirable that it is less than [0.001atomic%].
[0024] Moreover, the range which has the influence which nitrogen has on an interface from the interface of gate dielectric film and a silicon substrate was examined.
[0025] Drawing 1 is drawing which formed the gate dielectric film which consists of zirconic acid-ized film containing nitrogen on the silicon substrate, set the axis of abscissa as the distance to the location where a nitrogen content exceeds 0.1atomic(s)% from a silicon substrate surface, and set the axis of ordinate as the average coordination number in the interface structure of the silicon substrate of a field (100), and gate dielectric film.
[0026] If the location where a nitrogen content exceeds 0.1atomic(s)% separates 0.6nm or more from a silicon substrate surface so that clearly from drawing 1 , the average coordination number will begin to decrease gently. This Theoretical [J. of Philips of being structurally stable so that the average coordination number (NaV.) being close to 2.76 It is well in agreement with Vac.Sci.Tech B17(4) p1803(1999)]. Interface structure will become it unstable that the average coordination number is 2.9 or more, and interface state density will occur. Therefore, it is desirable for a nitrogen content to be less than [0.1atomic%] in 0.6nm in an interface with a silicon substrate to thickness of the gate dielectric film which consists of the metal oxide film or metal acid nitride containing nitrogen in this invention. Moreover, when the field whose nitrogen content is less than [0.1atomic%] is separated from an interface with a silicon substrate 1nm or more in thickness, in order that the average coordination number may begin to decrease more nearly gently, it is desirable. When 1.5 morenm or more is left, since the average coordination number does not change at the minimum value, it is more desirable almost to leave 1.5nm or more.
[0027] Drawing 2 is drawing which formed a metal oxide film (ZrO2) and the gate dielectric film which consists of a metal nitride (ZrN) formed on this metal oxide film on the silicon substrate, set the axis of abscissa as the distance from a silicon substrate surface to the interface of a metal nitride and a metal oxide film, and set the axis of ordinate as the average coordination number in the interface structure of the silicon substrate of a field (100), and a metal oxide film.
[0028] If distance with the interface of the interface of a silicon substrate and a metal oxide film, a

metal oxide film, and a metal nitride began to decrease gently by 0.6nm or more, it began to carry out asymptotic by 1nm or more and 1.5nm or more nitrated case is separated as shown in drawing 2, it will not change mostly. Therefore, in the case of this laminated structure, distance with the interface of the interface of a silicon substrate and a metal oxide film, a metal oxide film, and a metal nitride should just be 0.6nm or more. Moreover, it can obtain desirably that 1nm or more of structures [be / still more desirably / it / 1.5nm or more] is more stable, and a good interface property can be acquired.

[0029] The metal oxide film in which drawing 3 was formed on (a) p-type silicon substrate (aluminum 2O3), The C-V property of the capacitor structure which consists of polish recon formed on this metal oxide film, (b) It is the C-V property of the capacitor structure which consists of polish recon formed on the metal oxide film (aluminum 2O3) formed on the p-type silicon substrate, the metal nitride (AlN) formed on this metal oxide film, and this metal nitride.

[0030] the direction which does not contain the nitrogen shown in (a) so that drawing 3 may show -- a flat band shift (deltaVfb) -- about 0.68 -- it is V. the way with the diffusion barrier layer containing the nitrogen shown by (b) on the other hand -- a flat band shift (deltaVfb) -- about 0.15 -- it was set to V and the flat band shift was a value small enough. This is the result of diffusion of Lynn (P) contained in polish recon being controlled by the diffusion barrier layer containing nitrogen, and shows that sufficient diffusion barrier property is obtained.

[0031] As mentioned above, by preparing the diffusion barrier layer which consists of a metallic oxide which contains nitrogen near the interface with the gate electrode in the gate dielectric film which consists of a metallic oxide, a flat band shift can be made small and a good silicon interface property can be realized.

[0032] Moreover, if nitriding treatment is carried out and nitrogen is added after making silicon contain in this gate dielectric film, Si in gate dielectric film will be absorbed by strong association of Si-N, and the silicone content near the interface with a silicon substrate will increase relatively. Near the interface with a silicon substrate, a silicone content with good electrical characteristics serves as a high metallic oxide by carrying out like this, and the nitrogen content which prevents diffusion serves as a high metallic oxide near the interface with a gate electrode.

[0033] Drawing 4 is the sectional view of the MIS mold field-effect transistor which has the gate structure concerning the operation gestalt of this invention.

[0034] This MIS mold field-effect transistor possesses the p-type silicon substrate 101, the gate dielectric film 103 which consists of a metal oxide film containing the nitrogen formed on this silicon substrate 101, and the gate electrode which consists of polish recon formed on this gate dielectric film. The nitrogen content in 0.6nm in thickness from an interface with the silicon substrate 101 in gate dielectric film 103 is less than [0.1atomic%]. Moreover, the nitrogen content in 0.6nm in thickness from an interface with the gate electrode 104 in gate dielectric film 103 is 10atomic(s)%. Moreover, as a gate electrode 104, the electrode of polish recon which has metals, such as TiN, TaN, W, Nb, Zr, Ru, and Ru oxide, to replace may be used.

[0035] Moreover, the source / drain field 105 where n mold impurity was introduced and which is a diffusion layer are formed in the location which sandwiches the gate electrode 104 in a silicon substrate 101. The gate side attachment wall 106 which consists of a silicon nitride is formed in the side attachment wall of the gate electrode 104. 107 is an interlayer insulation film which consists of silicon oxide, and the aluminum wiring 108 is connected to the gate electrode 104, and the source / drain field 105 through the contact hole prepared in the interlayer insulation film 107. This formed MIS mold field-effect transistor is detached by the component by the component isolation region 102, respectively.

[0036] When the gate length of this MIS mold field-effect transistor was formed as 50nm and the check of operation was carried out, leakage current was controlled, the flat-band-voltage shift was small, and mobility was high.

[0037] Drawing 5 is a sectional view for explaining the concrete formation approach of the gate dielectric film 103 of the MIS mold field-effect transistor shown in drawing 4.

[0038] First, as shown in drawing 5 (a), the slot for isolation is formed by reactive ion etching on the p-type silicon substrate 101 of field bearing (100), specific resistance 4 - 6-ohmcm. Then, the component isolation region 102 is formed by embedding the LP(low pressure)-TEOS film, for example.
[0039] Next, as shown in drawing 5 (b), the metallic oxide 109 which consists of HfO2 at the substrate temperature of 400 degrees C is formed on a silicon substrate 101 by 5nm in thickness among the ambient atmosphere of 1x104Pa of oxygen tension, using the laser ablation forming-membranes method. By using the laser ablation forming-membranes method, by carrying out optical pumping of the material gas, each element has sufficient energy and can form the film with few gaps in the presentation ratio of a metal atom and an oxygen atom. If there is no gap in a presentation ratio, it will be hard to produce a dangling bond, and it works in favor of a defect forming few insulator layers.
[0040] Moreover, the spatter forming-membranes method may be used for a change of the laser ablation forming-membranes method, and a metallic oxide 109 may be formed in it. After depositing the metallic oxide 109 which consists of HfO2 at the substrate temperature of 300 degrees C among the ambient atmosphere of oxygen tension 40mtorr on a silicon substrate 101 in 3nm in thickness in this case, it is desirable to anneal in a 600 degrees C - 800 degrees C oxygen ambient atmosphere, and to carry out eburnation of the metallic oxide 109.
[0041] Moreover, a metallic oxide 109 may be formed using vacuum deposition. After depositing the metallic oxide which consists of HfO2 at the substrate temperature of 200 degrees C on a silicon substrate 101 in 4nm in thickness in this case, it is desirable to anneal in a 600 degrees C - 800 degrees C oxygen ambient atmosphere, and to carry out eburnation of the metallic oxide 109.
[0042] Moreover, a metallic oxide 109 may be formed using the CVD forming-membranes method. In this case, for example, the mixed gas of C16H36HfO4 gas and oxygen gas, mixed gas of HfCl4 gas, NH3 gas, and oxygen gas, or mixed gas of Hf(SO4)2 gas, NH3 gas, and oxygen gas etc., The mixed gas of the gas containing Hf, and oxygen gas by the pressure of 1Pa - 104Pa, and the flow rate of 1sccm - 1000sccm After supplying and exhausting, respectively and depositing substrate temperature in a temperature requirement with a room temperature of about 800 degrees C, it anneals in a 600 degrees C - 900 degrees C oxygen ambient atmosphere, and it is a metallic oxide. It is desirable to carry out eburnation of 109.
[0043] Next, as shown in drawing 5 (c), by heating in the ambient atmosphere of NO gas and NH3 gas, it nitrides near the front face of a metallic oxide 109, and the diffusion barrier layer 116 is formed. The nitrogen content of the diffusion barrier layer 116 at this time was about 10 atomic(s)%.
[0044] Moreover, using nitrogen IMPURA as an approach of forming the diffusion barrier layer 116 which consists of a metallic oxide containing nitrogen, a nitrogen atom is injected only into the front face of a metallic oxide 109, and a nitrogen atom may be stabilized by rapid heating (RTA).
[0045] Moreover, excitation (radical) nitrogen is irradiated on the front face of a metallic oxide 109, and the diffusion barrier layer 116 may be formed. Since there is an inclination for nitriding to progress from the front face of a metallic oxide 109, especially by the approach of irradiating excitation nitrogen, it is effective especially when it is desirable to nitride only a surface layer.
[0046] Moreover, instead of forming the diffusion barrier layer 116 which consists of a metallic oxide containing nitrogen, as shown in drawing 5 (d), in 300 degrees C - 500 degrees C and the pressure of 1Pa - 104Pa, the CVD silicon nitride 111 of 1nm - 3nm of thickness is deposited using the mixed gas of SiH4 gas diluted with nitrogen gas, and NH3 gas, and it is good also considering this as a diffusion barrier layer. The technique of making only the front face of a metallic oxide 109 diffuse nitrogen, and making it segregate by using rapid overheating (RTA) for the silicon nitride 111 further at this time is also effective.
[0047] Moreover, a nitriding metallic oxide like HfN is deposited instead of the silicon nitride 111 using a spatter, vacuum evaporationo, the laser ablation method, etc., and it is good also considering this as a diffusion barrier layer.
[0048] Next, by the chemical-vapor-deposition method, the polish recon film is deposited on the

whole surface, patterning of this polish recon film is carried out, and the gate electrode 104 is formed. Then, for example in 450 degrees C and the pressure of 1Pa - 104Pa, the mixed gas of SiH4 gas diluted with nitrogen gas and NH3 gas is used, for example, it is the 5nm - 200nm CVD silicon nitride 106. It deposits.

[0049] Like the production process of the usual MIS mold field-effect transistor, future processes perform the ion implantation of arsenic by acceleration voltage 20KeV and dose 1x1015cm-2, and form the source / drain field 105. Then, by the chemical-vapor-deposition method, the interlayer insulation film 107 which consists of silicon oxide is deposited on the whole surface, and opening of the contact hole is carried out to this interlayer insulation film 107. Then, aluminum film is deposited on the whole surface by the spatter, patterning of this aluminum film is carried out by reactive ion etching, and wiring 108 is formed. The MIS mold field-effect transistor shown in drawing 4 can be formed through such a process.

[0050] Next, with reference to drawing 6 , the another manufacture approach in the gate dielectric film 103 of the MIS mold field-effect transistor shown in drawing 4 is explained. The metallic oxide explained by drawing 4 is made to contain silicon here.

[0051] First, as shown in drawing 6 (a), the slot for isolation is formed by reactive ion etching on the p-type silicon substrate 101 of field bearing (100), specific resistance 4 - 6-ohmcm. Then, the component isolation region 102 is formed by embedding the LP(low pressure)-TEOS film, for example.

[0052] Next, as shown in drawing 6 (b), Hf silicate oxide 113 is formed on a silicon substrate 101 by 5nm in thickness among the ambient atmosphere of 1x104Pa of oxygen tension using the target which consists of substrate temperature of 400 degrees C by Hf, Si, and the oxygen atom, using the laser ablation forming-membranes method. By using the laser ablation forming-membranes method, by carrying out optical pumping of the material gas, each element has sufficient energy and can form the film with few gaps in the presentation ratio of a metal atom and an oxygen atom. If there is no gap in a presentation ratio, it will be hard to produce a dangling bond, and it works in favor of a defect forming few insulator layers.

[0053] Moreover, the spatter forming-membranes method may be used for a change of the laser ablation forming-membranes method, and the metal silicate oxide 113 may be formed in it. After depositing Hf metal, Hf silicide, or Hr silicate on a silicon substrate 101 at the substrate temperature of 300 degrees C among the ambient atmosphere of oxygen tension 40mtorr in this case, it can anneal in a 600 degrees C - 800 degrees C oxygen ambient atmosphere, and Hf silicate oxide 113 can be formed.

[0054] Moreover, the metal silicate oxide 113 may be formed using vacuum deposition. After depositing Hf metal or Hf silicide on a silicon substrate 101 by 4nm in thickness at the substrate temperature of 200 degrees C in this case, it can anneal in a 600 degrees C - 800 degrees C oxygen ambient atmosphere, and Hf silicate oxide 113 can be formed.

[0055] Moreover, the metal silicate oxide 113 may be formed using the CVD forming-membranes method. In this case, for example, the mixed gas of C16H36HfO4 gas, mono-silane (SiH4) gas, and nitrogen gas, mixed gas of HfCl4 gas, NH3 gas, and mono-silane (SiH4) gas, or mixed gas of Hf (SO4)2 gas, NH3 gas, and mono-silane (SiH4) gas etc., The mixed gas of the gas containing Hf, and the gas containing silicon by the pressure of 1Pa - 104Pa, and the flow rate of 1sccm - 1000sccm After supplying and exhausting, respectively and depositing substrate temperature in a temperature requirement with a room temperature of about 800 degrees C, it can anneal in a 600 degrees C - 900 degrees C oxygen ambient atmosphere, and the metal silicate oxide 113 can be formed.

[0056] Moreover, as an option which forms the metal silicate oxide film 113, as shown in drawing 6 (c), SiO2 film with a thickness of 1nm - about 4nm is formed for a silicon substrate 101 on a silicon substrate 101 by heating, BOX (combustion oxidation), or CVD in an oxygen ambient atmosphere. Next, the film which has a metallic element on a silicon substrate 101 with vacuum deposition is deposited using the target which contained Hf metal target or Hf metal atom, and the silicon atom at least, for example.

[0057] Then, for example, 400 degrees C - 900 degrees C heating may perform the process which diffuses a metallic element in SiO2 film at least in a vacuum or nitrogen, and the metal silicate oxide film 113 which contains Hf atom, a silicon atom, and an oxygen atom at least on a silicon substrate 101 may be formed.
[0058] According to the above process, after forming the metal silicate oxide film 113, as shown in drawing 6 (c), by heating in the ambient atmosphere of NO gas and NH3 gas, it nitrides near the front face of the metal silicate oxide film 113, and the diffusion barrier layer 116 is formed. The nitrogen content of the diffusion barrier layer 116 at this time was about 10 atomic(s)%.
[0059] Moreover, using nitrogen IMPURA as an approach of forming the diffusion barrier layer 116 which consists of metal silicate oxide containing nitrogen, a nitrogen atom is injected only into the front face of metal silicate oxide 113, and a nitrogen atom may be stabilized by rapid heating (RTA).
[0060] Moreover, excitation (radical) nitrogen is irradiated on the front face of metal silicate oxide 113, and the diffusion barrier layer 116 may be formed. Since there is an inclination for nitriding to progress from the front face of the metal silicate oxide 113, especially by the approach of irradiating excitation nitrogen, it is effective especially when it is desirable to nitride only a surface layer.
[0061] Moreover, instead of forming the diffusion barrier layer 116 which consists of metal silicate oxide containing nitrogen, as shown in drawing 6 (d), in 300 degrees C - 500 degrees C and the pressure of 1Pa - 104Pa, the CVD silicon nitride 111 of 1nm - 3nm of thickness is deposited using the mixed gas of SiH4 gas diluted with nitrogen gas, and NH3 gas, and it is good also considering this as a diffusion barrier layer. The technique of making only the front face of the metal silicate oxide 113 diffuse nitrogen, and making it segregate by using rapid overheating (RTA) for the silicon nitride 111 further at this time is also effective.
[0062] Moreover, a nitriding metallic oxide like HfN is deposited instead of the silicon nitride 111 using a spatter, vacuum evaporationo, the laser ablation method, etc., and it is good also considering this as a diffusion barrier layer.
[0063] Next, by the chemical-vapor-deposition method, the polish recon film is deposited on the whole surface, patterning of this polish recon film is carried out, and the gate electrode 104 is formed. Then, for example in 450 degrees C and the pressure of 1Pa - 104Pa, the mixed gas of SiH4 gas diluted with nitrogen gas and NH3 gas is used, for example, it is the 5nm - 200nm CVD silicon nitride 106. It deposits.
[0064] Like the production process of the usual MIS mold field-effect transistor, future processes perform the ion implantation of arsenic by acceleration voltage 20KeV and dose 1x1015cm-2, and form the source / drain field 105. Then, by the chemical-vapor-deposition method, the interlayer insulation film 107 which consists of silicon oxide is deposited on the whole surface, and opening of the contact hole is carried out to this interlayer insulation film 107. Then, aluminum film is deposited on the whole surface by the spatter, patterning of this aluminum film is carried out by reactive ion etching, and wiring 108 is formed. The MIS mold field-effect transistor shown in drawing 4 can be formed through such a process.
[0065] As mentioned above, although some operation gestalten of this invention have been shown, this invention is not limited to the above-mentioned range.
[0066] For example, after using the target containing a metal atom and an oxygen atom and making an insulator layer deposit by vacuum deposition or the spatter, irradiating excitation oxygen, it may expose to the ambient atmosphere containing a nitrogen atom, and nitrogen may be made to permeate a gate-dielectric-film-front-face.
[0067] Moreover, the SiO2/Si interface structure, or the silicate / Si interface structure which does not contain nitrogen may be formed in a silicon substrate surface by forming a metal nitride or a metal acid nitride, and carrying out ion in plastic **** heating of the oxygen at an interface with a silicon substrate.
[0068]
[Effect of the Invention] As described above, by this invention, by forming the diffusion barrier layer containing nitrogen in the part in the gate dielectric film which consists of a metallic oxide, diffusion

of the impurity metallurgy group atom from a gate electrode can be prevented, and the MIS mold field-effect transistor which can control a flat-band-voltage shift and the fall of mobility, and its manufacture approach can be offered.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] Drawing which formed the gate dielectric film which consists of zirconic acid-ized film containing nitrogen on the silicon substrate, set the axis of abscissa as the distance to the location where a nitrogen content exceeds 0.1atomic(s)% from a silicon substrate surface, and set the axis of ordinate as the average coordination number in the interface structure of the silicon substrate of a field (100), and gate dielectric film.
[Drawing 2] Drawing which formed a metal oxide film (ZrO2) and the gate dielectric film which consists of a metal nitride (ZrN) formed on this metal oxide film on the silicon substrate, set the axis of abscissa as the distance from a silicon substrate surface to the interface of a metal nitride and a metal oxide film, and set the axis of ordinate as the average coordination number in the interface structure of the silicon substrate of a field (100), and a metal oxide film.
[Drawing 3] (a) The metal oxide film formed on the p-type silicon substrate (aluminum 2O3), The C-V property of the capacitor structure which consists of polish recon formed on this metal oxide film, (b) Drawing showing the C-V property of the capacitor structure which consists of polish recon formed on the metal oxide film (aluminum 2O3) formed on the p-type silicon substrate, the metal nitride (AlN) formed on this metal oxide film, and this metal nitride.
[Drawing 4] The sectional view of the MIS mold field-effect transistor which has the gate structure concerning the operation gestalt of this invention.
[Drawing 5] The sectional view for explaining the concrete formation approach of the gate dielectric film of the MIS mold field-effect transistor concerning the operation gestalt of this invention.
[Drawing 6] The sectional view for explaining the production process of the MIS mold field-effect transistor concerning the operation gestalt of this invention.
[Description of Notations]
101 -- Silicon substrate
102 -- Component isolation region
103 -- Gate dielectric film
104 -- Gate electrode
105 -- The source / drain field
106 -- Metal oxide film containing nitrogen
107 -- Interlayer insulation film
108 -- aluminum wiring
109 -- Metallic-oxide film
111 -- Metal silicate oxide film containing nitrogen
113 -- Metal silicate oxide film
114 -- SiO2 film
115 -- Film containing ****

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The MIS mold field-effect transistor which possesses the gate dielectric film which becomes at least the part formed on the silicon substrate and said silicon substrate from the metallic-oxide film or metal acid nitride film containing nitrogen, and the gate electrode formed on said gate dielectric film, and is characterized by the nitrogen content near the interface with said silicon substrate being lower than other parts of said gate dielectric film among said metallic-oxide film or the metal acid nitride film.
[Claim 2] The MIS mold field-effect transistor according to claim 1 characterized by the nitrogen content near the interface with said silicon substrate being less than [0.1atomic%] among said gate dielectric film.
[Claim 3] It is the MIS mold field-effect transistor according to claim 1 characterized by being 0.6nm or less in thickness near the interface with said silicon substrate from said silicon substrate among said gate dielectric film.
[Claim 4] The MIS mold field-effect transistor according to claim 1 characterized by a nitrogen content with a thickness of 0.6nm or less being more than 10atomic% from an interface with said gate electrode among said gate dielectric film.
[Claim 5] A silicon substrate and the gate dielectric film which becomes at least the part formed on said silicon substrate from the metallic oxide containing nitrogen, The gate electrode formed on said gate dielectric film is provided, and the nitrogen content in a field with a thickness of 0.6nm is less than [0.1atomic%] from an interface with said silicon substrate among said gate dielectric film. And the MIS mold field-effect transistor characterized by the nitrogen content in a field with a thickness of 0.6nm being more than 10atomic% at least from an interface with said gate electrode among said gate dielectric film.
[Claim 6] The MIS mold field-effect transistor according to claim 1 to 5 characterized by silicon containing in said gate dielectric film.
[Claim 7] The MIS mold field-effect transistor characterized by providing a silicon substrate, the gate dielectric film which consists of a metallic oxide formed on said silicon substrate, the silicon nitride formed on said gate dielectric film, and the gate electrode formed on said silicon nitride.
[Claim 8] Said metallic oxide is an MIS mold field-effect transistor according to claim 1 to 7 characterized by including Zr, Hf, La, Ce, Ti, aluminum, Y, Mg, Ta, or Bi.
[Claim 9] The manufacture approach of the MIS mold field-effect transistor according to claim 1 to 6 characterized by introducing nitrogen into said metallic oxide by being exposed into heat treatment or excitation nitrogen in nitrogen-gas-atmosphere mind.
[Claim 10] The manufacture approach of the MIS mold field-effect transistor according to claim 1 to 6 characterized by introducing nitrogen into said metallic oxide by being exposed into heat treatment or excitation nitrogen in nitrogen-gas-atmosphere mind before forming said gate electrode.

[Translation done.]